Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 24 (cancelled).

Claim 25. (original) A system adapted for coupling to a switch fabric and a central processor, the system comprising:

a first integrated circuit having a first bus interface, a second bus interface, and a control interface, a data path extending from the first bus interface, through segmentation circuitry on the first integrated circuit, through reassembly circuitry on the first integrated circuit, and to the second bus interface;

a second integrated circuit that is substantially structurally identical to the first integrated circuit, the second integrated circuit having a first bus interface, a second bus interface, and a control interface, the second integrated circuit having a data path extending from the first bus interface, through segmentation circuitry on the second integrated circuit, through reassembly circuitry on the second integrated circuit, and to the second bus interface; and

a control integrated circuit having a first control interface coupled to the control interface of the first integrated circuit, having a second control interface coupled to the control interface of the second integrated circuit, and having a third interface adapted for coupling to the central processor, the control integrated circuit controlling a first flow of network information out of the first integrated circuit, the first flow passing over the data path of the first integrated circuit, the control integrated circuit controlling a second flow of network information out of the second integrated circuit, the second flow passing over the data path of the second integrated circuit, wherein in operation either the first bus interface of the first integrated circuit and the first bus interface of the second integrated circuit are coupled to the switch fabric or the second bus

interface of the first integrated circuit and the second bus interface of the second integrated circuit are coupled to the switch fabric.

Claim 26. (original) The system of Claim 25, wherein network information of the first flow is stored by the first integrated circuit in a plurality of first buffers, all of the first buffers having the same size, the control integrated circuit controlling the first flow of network information out of the first integrated circuit by supplying an indication of a first buffer to the first integrated circuit via the control interface of the first integrated circuit such that the first integrated circuit retrieves the contents of the first buffer and outputs the contents from the first integrated circuit, and

wherein network information of the second flow is stored by the second integrated circuit in a plurality of second buffers, all of the second buffers having the same size, the control integrated circuit controlling the second flow of network information out of the second integrated circuit by supplying an indication of a second buffer to the second integrated circuit via the control interface of the second integrated circuit such that the second integrated circuit retrieves the contents of the buffer and outputs the contents from the second integrated circuit.

Claim 27. (original) The system of Claim 25, wherein the system can supply network information to the switch fabric at a maximum system data throughput rate, and wherein the data path through the first integrated circuit has a maximum data throughput rate, and wherein the data path through the second integrated circuit has a maximum data throughput rate, the maximum system data throughput rate being greater than the maximum data throughput rate of the first integrated circuit and being greater than the maximum data throughput rate of the second integrated circuit.

Claim 28. (original) The system of Claim 25, wherein the system can receive network information from the switch fabric at a maximum system data throughput rate, and wherein the data path through the first integrated circuit has a maximum data throughput rate, and wherein the data path through the second integrated circuit has a maximum data throughput rate, the maximum system data throughput rate being greater than the maximum data throughput rate of

the first integrated circuit and being greater than the maximum data throughput rate of the second integrated circuit.

Claims 29 to 44 (cancelled)

Claim 45. (previously presented) The system of Claim 25, further comprising:

an aggregation integrated circuit having a first bus interface coupled to the second bus interface of the first integrated circuit, a second bus interface coupled to the second bus interface of the second integrated circuit, and a third bus interface through which the first and second flows of network information pass.

Claim 46. (previously presented) The system of Claim 45, wherein the first and second flows of network information pass from the third bus interface of the aggregation integrated circuit to the switch fabric.

Claim 47. (previously presented) The system of Claim 45, wherein the first and second flows of network information pass from the third bus interface of the aggregation integrated circuit to a framer/mapper.

Claim 48. (previously presented) The system of Claim 25, further comprising:

a distribution integrated circuit having a first bus interface coupled to the first bus interface of the first integrated circuit, a second bus interface coupled to the first bus interface of the second integrated circuit, and a third bus interface into which the first and second flows of network information pass.

Claim 49. (previously presented) The system of Claim 48, wherein the first and second flows of network information pass from a classification engine and into the third bus interface of the distribution integrated circuit.

Claim 50. (previously presented) The system of Claim 48, wherein the first and second flows of network information pass from the switch fabric and into the third bus interface of the distribution integrated circuit.

Claim 51. (currently amended) The system of Claim 48, wherein the distribution integrated circuit receives a packet via the third bus interface of the distribution integrated circuit, wherein the distribution integrated circuit adds a sequence number to the packet, and wherein the distribution integrated circuit outputs the packet with the sequence number to a selected ~~on~~ one of the first integrated circuit and the second integrated circuit.

Claim 52. (previously presented) The system of Claim 48, wherein the distribution integrated circuit receives a flow of packets on the third bus interface, wherein the distribution integrated circuit adds a sequence number to each packet in the flow such that each respective packet of the flow has a sequence number that is greater than the sequence number of the previous packet in the flow, the distribution integrated circuit outputting the flow of packets having the sequence numbers.

Claim 53. (previously presented) A system, comprising:

a distribution integrated circuit having a first bus interface, a second bus interface, and a third bus interface, the distribution integrated circuit receiving a plurality of flows of packets via the third bus interface, the distribution integrated circuit adding a sequence number to each of the packets of a flow such that each successive packet of a flow carries a sequence number that is greater than the sequence number of the previous packet in that flow;

a first integrated circuit having a first bus interface and a second bus interface, a data path extending from the first bus interface of the first integrated circuit, through segmentation circuitry on the first integrated circuit, through reassembly circuitry on the first integrated circuit, and to the second bus interface of the first integrated circuit, the first integrated circuit receiving a first packet containing a first sequence number from the distribution integrated circuit via the first bus interface of the first integrated circuit;

a second integrated circuit having a first bus interface and a second bus interface, the second integrated circuit being substantially structurally identical to the first integrated circuit, a data path extending from the first bus interface of the second integrated circuit, through segmentation circuitry on the second integrated circuit, through reassembly circuitry on the second integrated circuit, and to the second bus interface of the second integrated circuit, the second integrated circuit receiving a second packet containing a second sequence number from the distribution integrated circuit via the first bus interface of the second integrated circuit; and

a control integrated circuit coupled to the first integrated circuit and to the second integrated circuit, the first integrated circuit supplying the first sequence number to the control integrated circuit, the second integrated circuit supplying the second sequence number to the control integrated circuit, the control integrated circuit using the first and second sequence numbers to determine which packets of which flows have been received onto which of the first and second integrated circuits.

Claim 54. (previously presented) The system of Claim 53, wherein the first integrated circuit performs a lookup operation on the first packet and identifies a flow identifier associated with the first packet, the first integrated circuit supplying the flow identifier to the control integrated circuit, the control integrated circuit using both the flow identifier and the first sequence number in said determining of which packets of which flows have been received onto which of the first and second integrated circuits.

Claim 55. (previously presented) The system of Claim 53, wherein the control integrated circuit maintains a packet queue for each flow of the plurality of flows.

Claim 56. (previously presented) The system of Claim 53, wherein the control integrated circuit controls the first integrated circuit and the second integrated circuit such that the system performs traffic shaping and traffic metering.

Claim 57. (previously presented) The system of Claim 53, further comprising:

an aggregation integrated circuit that receives packets from the first and second integrated circuits and that outputs the packets, the packets received being packets of a particular flow, the packets of the particular flow having been received by the distribution integrated circuit in a particular order, wherein the aggregation integrated circuit outputs the packets of the particular flow from the aggregation integrated circuit in the same order in which the packets of the particular flow were received by the distribution integrated circuit.

Claim 58. (previously presented) A method, comprising:

receiving onto a first integrated circuit a flow of packets, the packets of the flow being received in a particular order, and distributing the packets from the first integrated circuit to a plurality of data path integrated circuits;

processing the packets on the plurality of data path integrated circuits, each of the data path integrated circuits having segmentation and reassembly circuitry, each of the plurality of data path integrated circuits being substantially structurally identical to every other of the plurality of data path integrated circuits; and

receiving onto a second integrated circuit the packets from the data path integrated circuits and aggregating the packets such that the packets are output from the second integrated circuit in the same order that they were received onto the first integrated circuit, wherein the first integrated circuit also receives a flow of cells, the cells being received in a particular order, the cells being processed by the plurality of data integrated circuits, the second integrated circuit outputting the cells in the same order that they were received onto the first integrated circuit, and wherein the first integrated circuit and the plurality of data path integrated circuits and the second integrated circuit are all disposed on a single line card.

Claims 59 to 60. (cancelled)